Amendments to the Specification:

Please replace paragraph [23] with the following amended paragraph:

--In operation, WR_DATA_IN received by the data bypass circuit 300 is driven through the input buffer 302 and is provided to the first input of the multiplexer 306. The WR_DATA_IN is also saved in the bypass register/FIFO 304. In response to an inactive ACT signal, an active EN signal is generated by the bypass select logic 308. The active EN signal enables output by the input/output buffer 310 and couples the output of the input buffer 302 to the input of the input/output buffer 310 through the multiplexer 306. As a result, the WR_DATA_IN is provided directly to the input of the input/output buffer 310 and the WR_DATA_IN is provided through the data bypass circuit 300 without any bypass. However, in response to an active ACT signal, the bypass select logic 308 generates an inactive EN signal, disabling the output function of the input/output buffer 310 and placing its output in a high-impedance state. Additionally, the inactive EN signal couples the input of the input/output buffer 310 to the output of the bypass register/FIFO 304. In this manner, the WR_DATA_IN is received by the data bypass circuit 300, stored by the bypass register/FIFO ~~306~~ 304, and applied to the input of the input/output buffer 310. However, due to the inactive state of the EN signal, the WR_DATA_IN is not provided as output data WR_DATA_OUT by the input/output buffer 310. As a result, the WR_DATA_IN is held in a bypass state until the ACT signal becomes inactive, at which time, the EN signal become active again, enabling the input/output buffer 310 to provide the WR_DATA_IN as WR_DATA_OUT data. The multiplexer 306 is also switched back to coupling the output of the input buffer 302 directly to the input of the input/output buffer 310 to allow WR_DATA_IN to pass through the data bypass circuit unhindered.--

Please replace paragraph [25] with the following amended paragraph:

--In Figure 4, it is assumed that the memory hub controller 128 has just issued read and write commands, with the read command sequenced prior to the write command. The read command is directed to the memory module 130b and the write command is directed to the memory module 130c. That is, the memory module to which data will be written is further downstream than the memory module from which data is read. In response to the read command, the memory hub 140b begins retrieving the read data (RD) from the memory device 148b, as indicated in Figure 4 by the "(1)". With the read command issued, the write command

is then initiated, and the write data (WD) is provided onto the high-speed link 134. However, since the memory hub controller 128 is expecting the RD to be returned from the memory module 130b, the memory hub 140a is directed to capture the WD in its data bypass circuit 286a. As a result, the ~~memory hub~~ data bypass circuit 286a captures the WD to clear the high-speed link 134, as indicated in Figure 4 by the "(2)", for the RD to be returned to the memory hub controller 128. When the memory hub 140b has retrieved the RD from the memory device 148b, and has indication from the memory hub 140a that the WD has been successfully captured by the data bypass circuit 286a, the RD is then provided to the memory hub controller 128 through the high-speed link 134, as indicated in Figure 4 by the "(3)" to complete the read request. Upon the RD passing through the memory hub 140a on its way to the memory hub controller 128, the memory hub 140a releases the WD from the data bypass circuit 286a to continue its way to the memory hub 140c. The WD is provided to the memory hub 140c through the high-speed link, which is now clear between the memory hub 140a and 140c. Upon reaching the memory hub 140c, the WD is written in the memory device 148c, as shown in Figure 4 by the "(4)".--